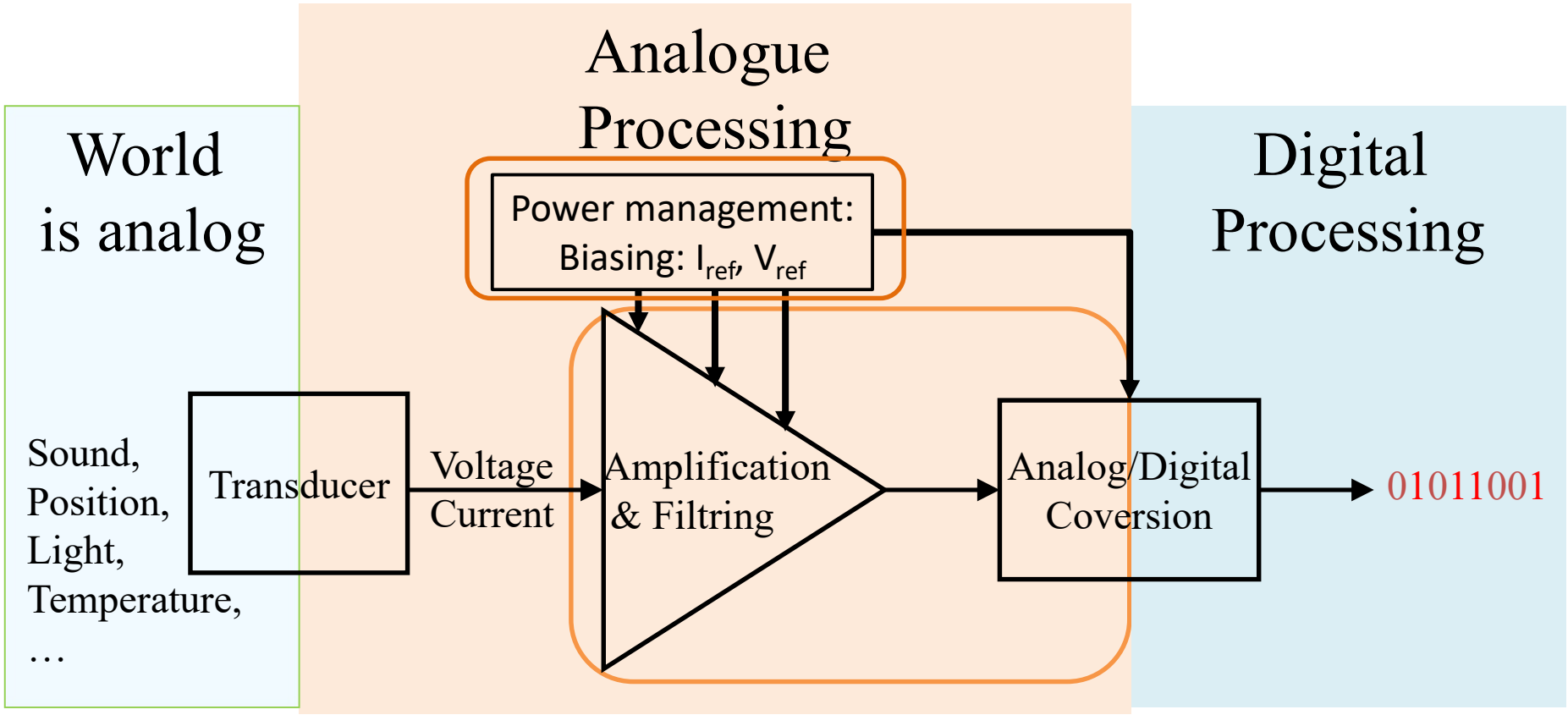
Operational Transconductance Amplifiers: OTA: Analysis, Design and Applications

Operational Transconductance Amplifiers A. KOUKAB

Contents

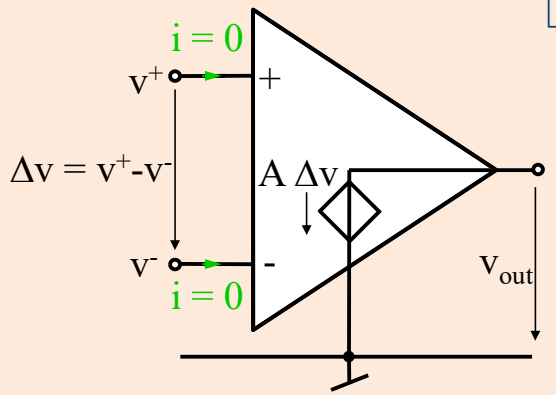
- Single vs Multistage OpAmp
- Basic and sophisticated OTA topologies
- DC analysis
  - LF Gain
  - Input and output dynamic range
  - Common mode rejection ratio: CMRR
  - Feedback for accuracy and stability
- Frequency analysis
  - Basic OTA analysis

Why OpAmp?


World
is analog
Analogue
Processing
Digital
Processing
Power management:
Biasing: I_{ref}, V_{ref}
Sound,
Position,
Light,
Temperature,
…
Transducer
Voltage
Current
Amplification
& Filtring
Analog/Digital
Coversion
01011001

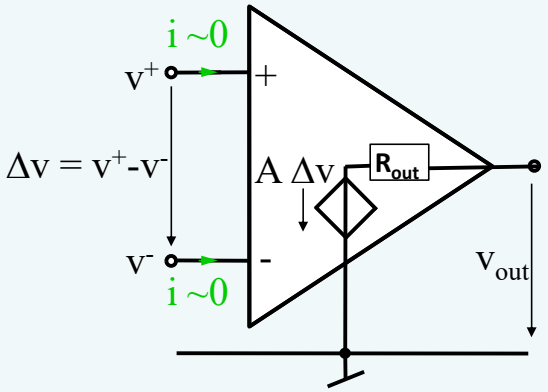
OpAmp: Evolution

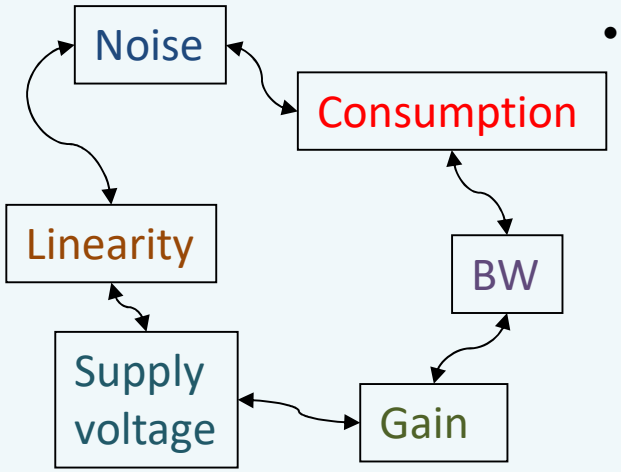
"General Purpose"



- Diff. gain $\rightarrow \infty$
- $R_{in} \rightarrow \infty$
- $R_{out} \rightarrow 0$
- High cost, power, area complexity…

ASICs "Specific Purpose"

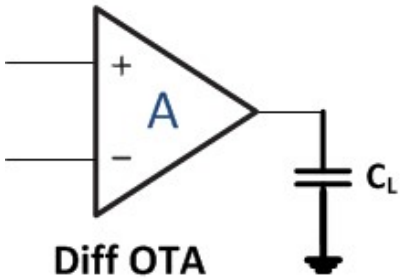




- Usually OTA designed with Relatively
  - High gain
  - High BW
  - Low Rout
    - (depend on the load)
  - High R_{in} (usually ∞ in CMOS)
  - Optimized cost, power, area complexity…

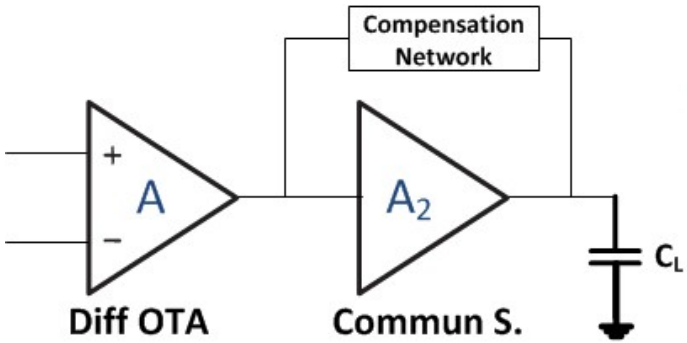
Single vs Multistage OpAmp

One-stage



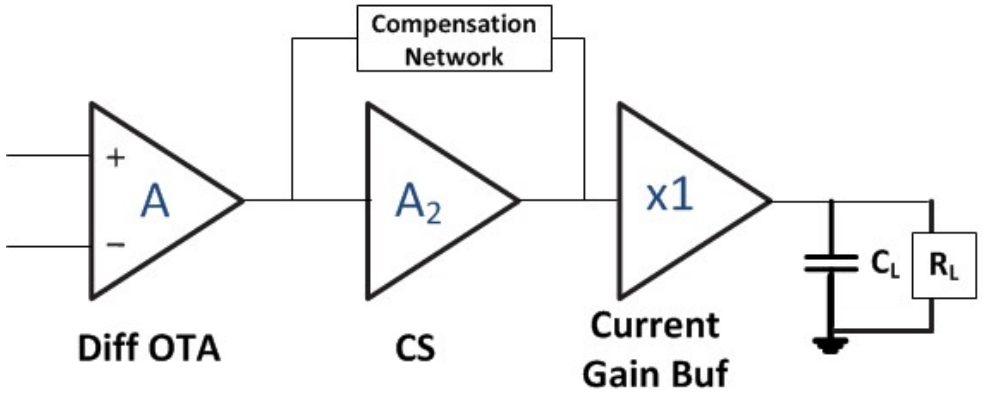
Gain boosting:
Cascode
Folded-Cascode
Auxiliary Amp.
Pb. Low swing

Two-stage



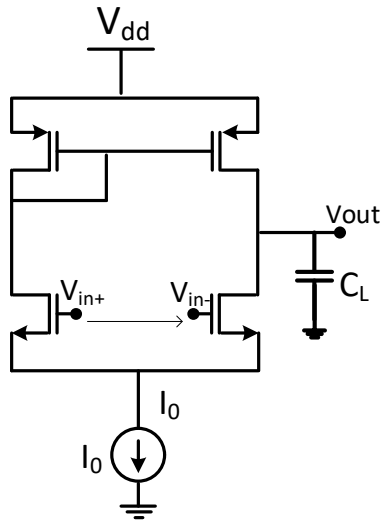
Compensation Tech. For stability
OTA for H. Gain
CS for H. Swing:

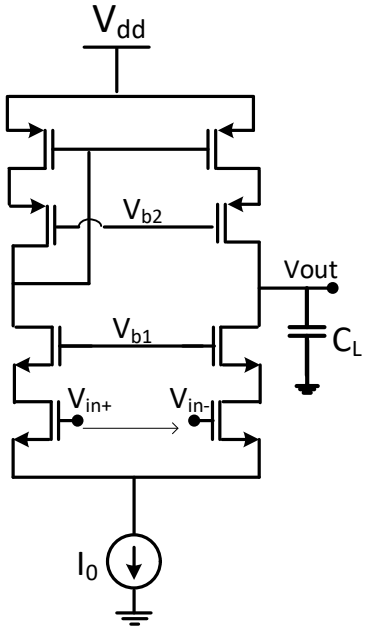
Three-stage

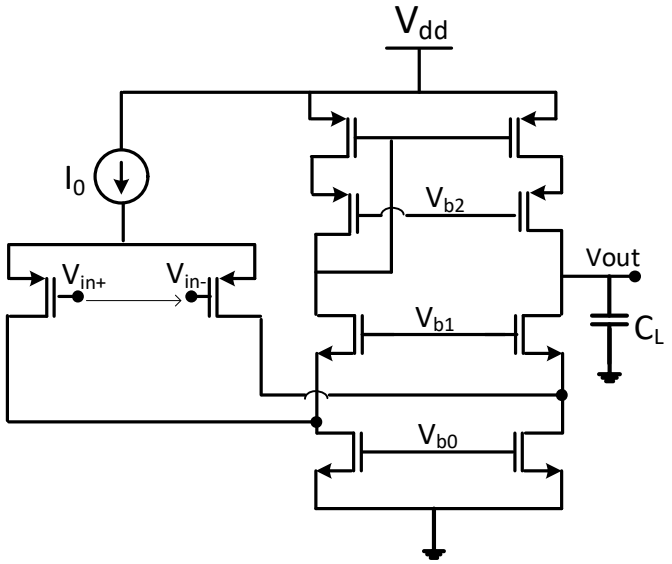


Current Gain Amplifier
Flower
Class AB

Class A: Basic OTA Structures







➢ **Simple OTA**
- Limited gain
- Large output swing

➢ **Telescopic OTA**
- Boosted gain
- Low output swing

➢ **Folded cascode OTA**
- Boosted gain
- Large output swing

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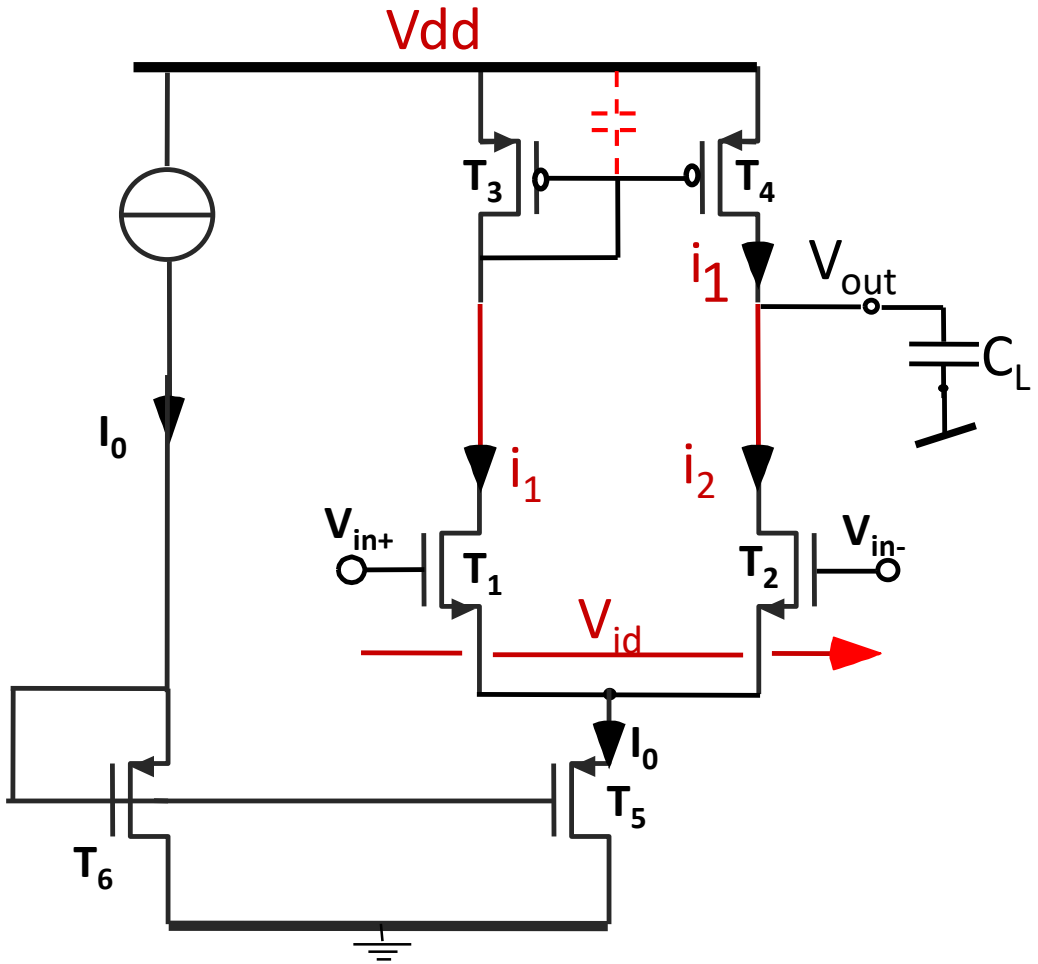
  - Feedback theory: Gain vs Band Width
  - Stability
  - Basic OTA analysis

Small signal (ac): LF Gain



$$V_{in+} = V_{ic} + v_{in+}$$

$$V_{in-} = V_{ic} + v_{in-}$$

V_{ic} is the input DC voltage and v_{in-}, v_{in+} the input ac diff. voltages

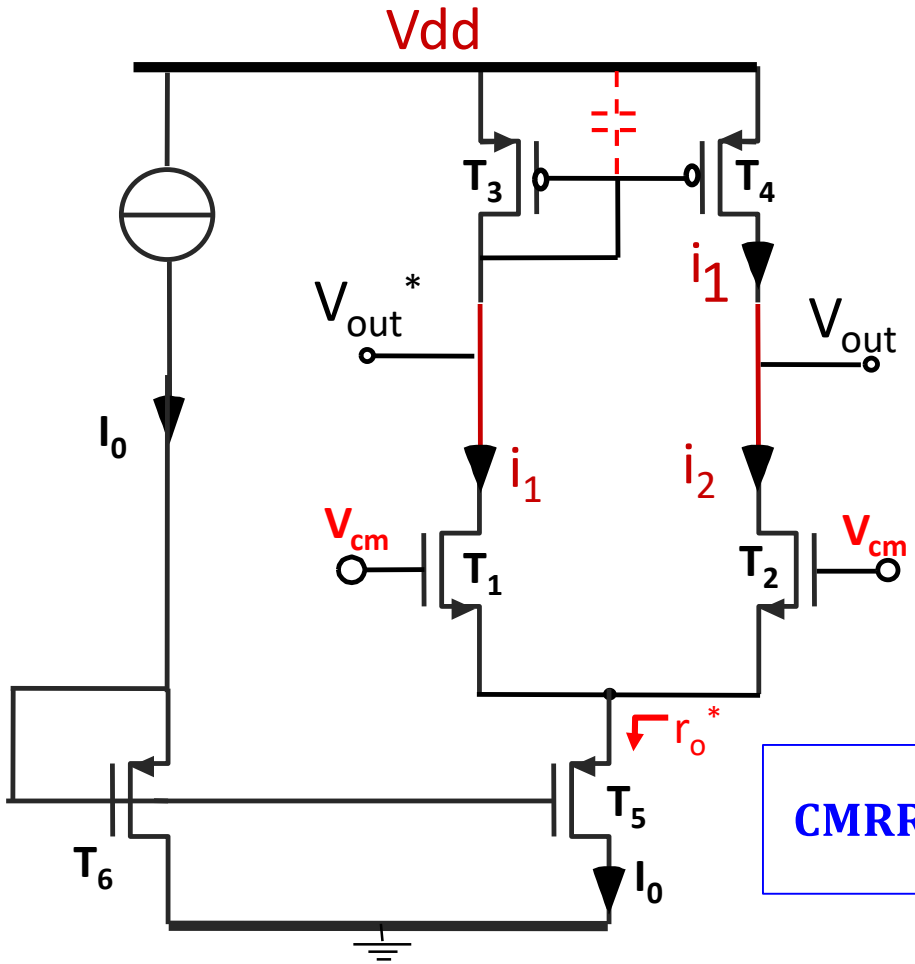
$$v_{id} = v_{in+} - v_{in-} = 2\, v_{in+}$$

$$\boxed{A = \frac{v_{out}}{v_{id}} = \frac{g_{m1,2}}{g_o}}$$

$$g_o = g_{ds4} + g_{ds2}$$

- Determine the gain at LF: $A_o = V_{out}/V_{id}$?
- What would be the impact of a resistive load?

Common Mode Gain (A_{cm}) & Rejection Ratio (CMRR)



Asymmetry + non-ideal current source
→ $A_{cm} \neq 0$

$$\mathbf{A_{cm} = \frac{v_{out}}{v_{cm}} \approx \frac{-1}{2g_{m3,4}r_o^*}}$$

$$\mathbf{CMRR = 20log\left|\frac{A_o}{A_{cm}}\right| \approx 20log\left(\frac{g_{m1,2}}{g_o}2g_{m3,4}r_o^*\right)}$$

- Determine A_{cm} due to the finite output resistance of the current source (suppose that the circuit is fully symmetric *(i.e. $v_{out,DC} = v_{out,DC}^*$)*
- Deduce CMRR

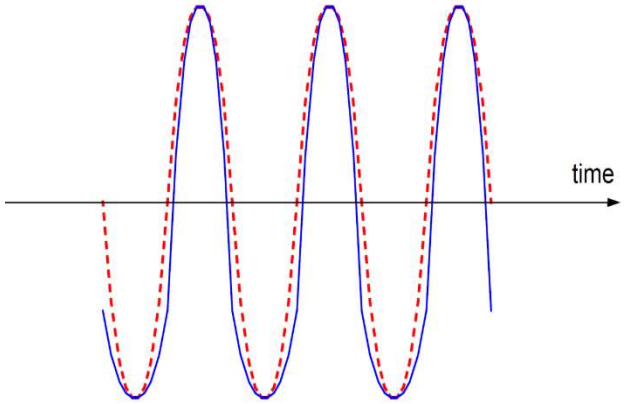
Analog Integrated Circuits Design (2024-25)

- MOST Operation, Modelling
  - 13-17 Sep MOSFETs: Operation and Modelling
  - 20-24 Sep Noise1 : (in time and frequency domains)
  - 27 Sep-1 Oct Noise-2 : (Analog circuits noise analysis)
- Voltage references and regulators
  - 04 Oct Current Sources and Mirrors
  - 08 Oct Voltage and Temperature independent References
  - 11 Oct Exercises
- OTA and Op-Amp Design
  - **15 Oct** OTA Analysis and Design (DC, AC, Stability …) (1)
  - 18-22-25 Oct Vacation
  - **29 Oct** OTA Analysis and Design (DC, AC, Stability …) (2)
  - **1 Nov Lab1-a: OTA Structural Design (g_m/I_D Methodology) theory**
  - **05 Nov Lab1-b: OTA Structural Design (g_m/I_D Methodology) Lab (CO5)**
  - 08 Nov: Multistage OTA (Stability and Frequency Compensation)
  - 12 Nov: Fully-Diff Amplifiers & CMFB
  - 15 Nov: Variability, offset and noise in OpAmp (1)
  - **19 Nov Lab2: Fully diff dolded cascode amplifier & its CMFB (CO5)**
  - 22 Nov: Variability, offset and noise in OpAmp (2)
  - 26 Nov: Rail to Rail input and output amplifiers
- Mixed-signal design
  - 29 Nov: Comparators
  - **03 Dec Lab3: Comparators (CO5)**
  - 06-10 Dec: AD and DA converters (introduction)
  - 13 Dec: Digital calibration of analog circuits
- 20 Dec General revision (zoom)

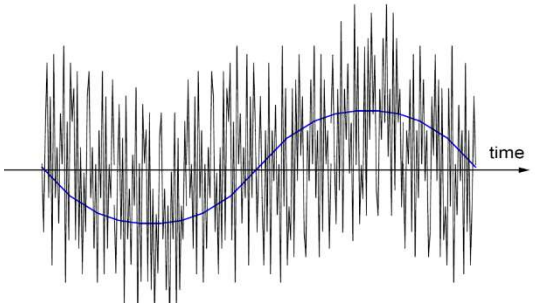
Output Dynamic Range

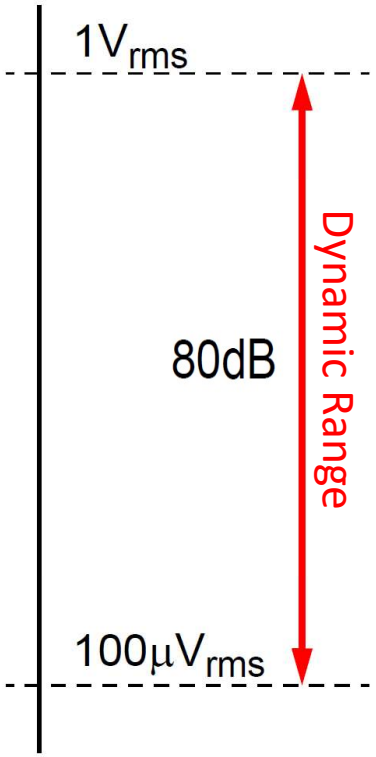
Dynamic Range = ratio between smallest and largest signal that the system can process

Distortion



Noise

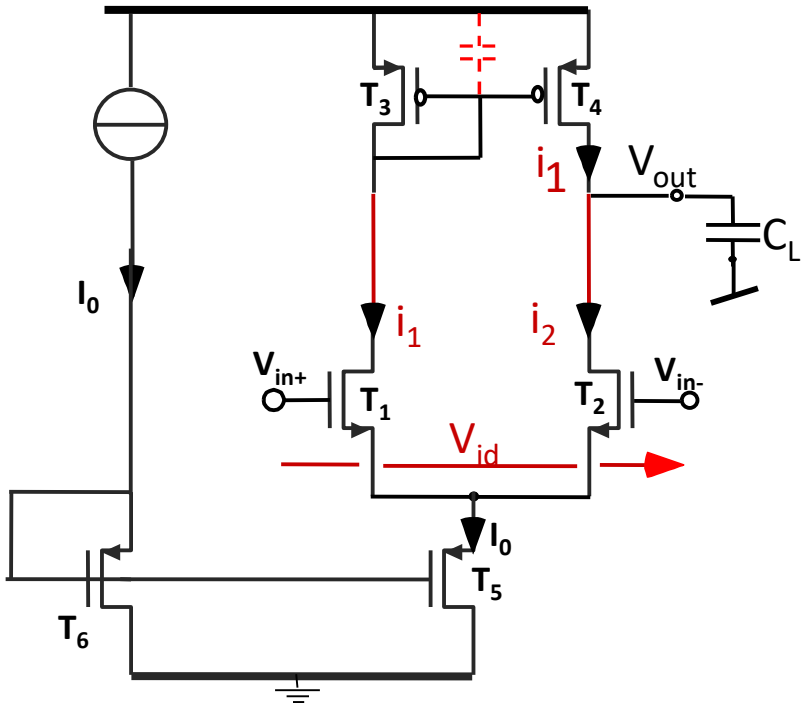




highest level, determined by distortion

lowest level, determined by noise

Large signal: Output Dynamic

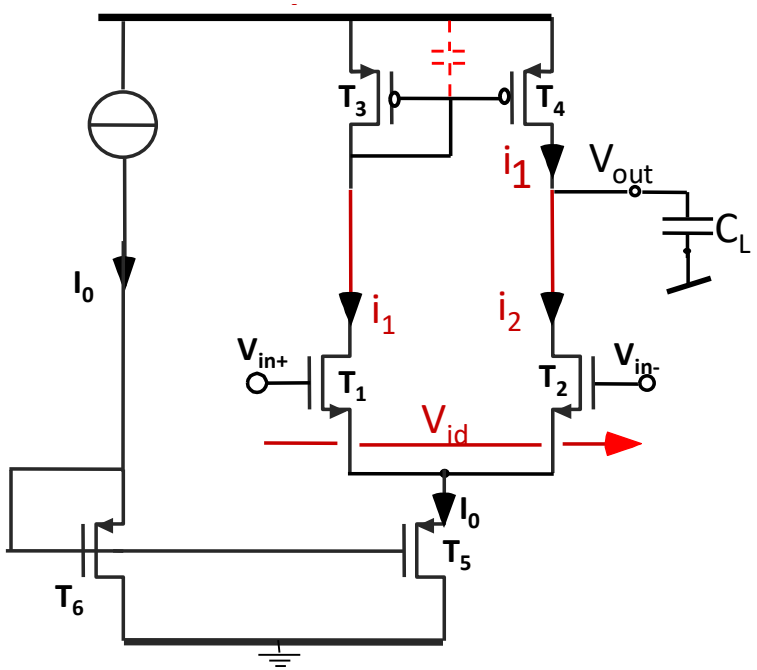


$$V_{out,max} = V_{dd} - V_{SD,sat4} = V_{dd} - (V_{SG4} - V_{Tp})$$

$$V_{out,min} = V_{D,sat2} = V_{in,DC} - V_{Tn}$$

- Determine $V_{out,max}$ and $V_{out,min}$? (all the transistors in strong inversion, $V_{in,DC}$ is set by a biasing circuit (e.g. to V_{DD} /2))

Large signal: T_1,T_2 in weak inversion

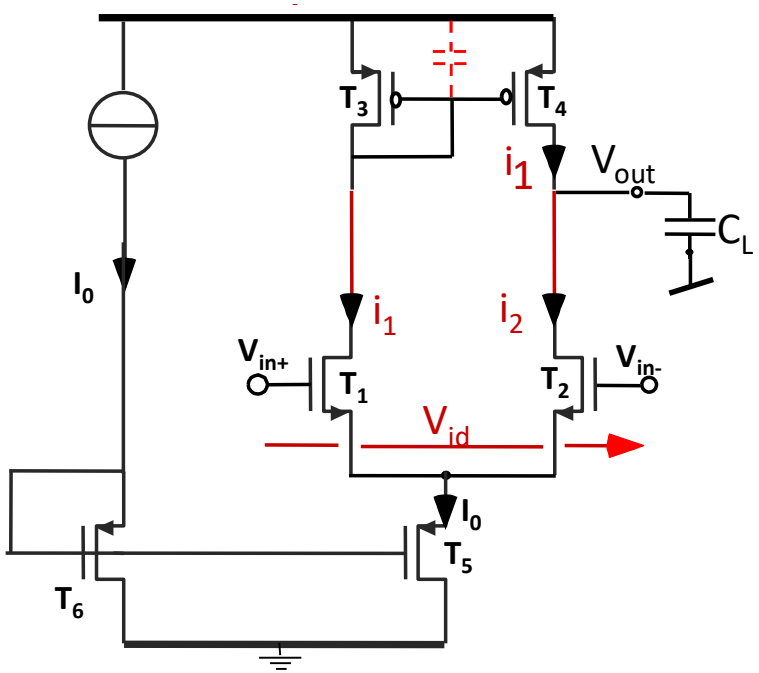


$$V_{out,max} = V_{dd} - V_{SD,sat4}$$
$$= V_{dd} - (V_{SG4} - V_{Tp})$$

$$V_{out,min} = V_{S2} + V_{DS,sat2}$$
$$\approx (V_{in,DC} - V_{SG2}) + 4U_T$$
$$\approx (V_{in,DC} - V_{Tn}) + 4U_T$$

- Determine $V_{out,max}$ and $V_{out,min}$ (T1 and T2 in weak inversion (wi))?

Large signal: Input Common Mode Range



$$V_{in+} = V_{ic} + v_{in+}$$

$$V_{in-} = V_{ic} + v_{in-} = V_{ic} - v_{in+}$$

$V_{ic,max} = Max(V_{cm})$
$= V_{dd} - V_{SG3} + V_{Tn}$

$V_{ic,min} = Min(V_{cm})$
$= V_{GS1} + V_{Dsat5}$
$= V_{GS1} + (V_{G5} - V_{T05})$

- Determine $V_{ic,max}$ and $V_{ic,min}$

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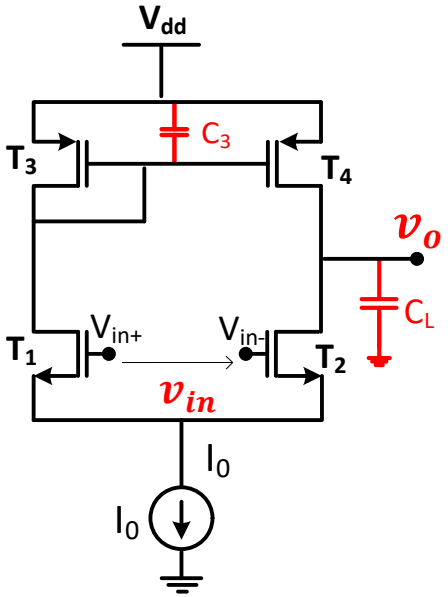
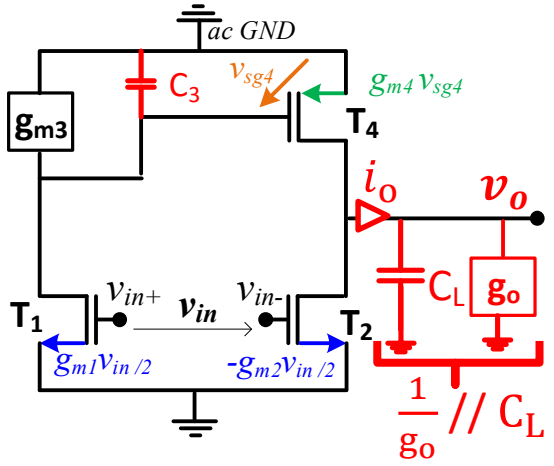
OTA- Frequency analysis



$$\mathbf{H(s)} = \frac{v_o}{v_{in}} = ?$$



ac model with parasitic capacitors

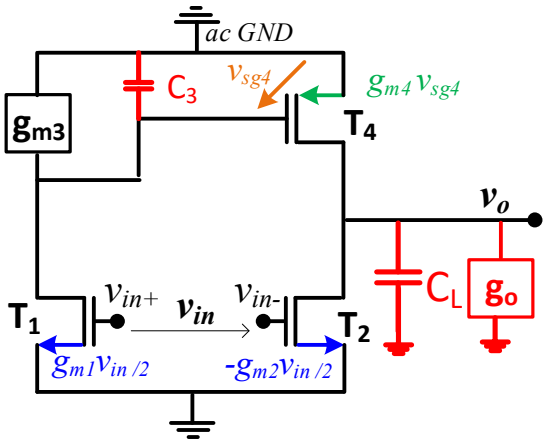
$$v_o = \underbrace{\left(g_{m4,3} v_{sg4} + \frac{g_{m2,1} v_{in}}{2}\right)}_{i_o} \underbrace{\frac{1}{g_o} \frac{1}{1 + s\frac{C_L}{g_o}}}_{\times \frac{1}{g_o} // C_L}$$

$$v_{sg4} = \underbrace{\frac{g_{m1,2} v_{in}}{2} \frac{1}{g_{m3,4}} \frac{1}{1 + s\frac{C_3}{g_{m3,4}}}}_{\frac{1}{g_{m3,4}} // C_3}$$

$g_{m1}=g_{m2}$ and $g_{m3}=g_{m4}$

$$v_o = \underbrace{\frac{g_{m1,2} v_{in}}{2} \left(1 + \frac{1}{1 + s\frac{C_3}{g_{m3,4}}}\right)}_{i_o} \frac{1}{g_o} \frac{1}{1 + s\frac{C_L}{g_o}}$$

OTA- Frequency analysis



$$v_o = \frac{g_{m1,2} v_{in}}{2}\left(1 + \frac{1}{1 + s\frac{C_3}{g_{m3,4}}}\right)\frac{1}{g_o}\frac{1}{1 + s\frac{C_L}{g_o}}$$

$$v_o = \frac{g_{m1,2} v_{in}}{2}\left(\frac{2 + s\frac{C_3}{g_{m3,4}}}{1 + s\frac{C_3}{g_{m3,4}}}\right)\frac{1}{g_o}\frac{1}{1 + s\frac{C_L}{g_o}}$$

A_o :DC Gain

Zero

$$\mathbf{H(s)} = \frac{v_o}{v_{in}} = \frac{\mathbf{g_{m2,1}}}{\mathbf{g_o}}\left(\frac{\mathbf{1 + s\frac{C_3}{2g_{m3,4}}}}{\left(\mathbf{1 + s\frac{C_3}{g_{m3,4}}}\right)\left(\mathbf{1 + s\frac{C_L}{g_o}}\right)}\right)$$

N Dom Pole

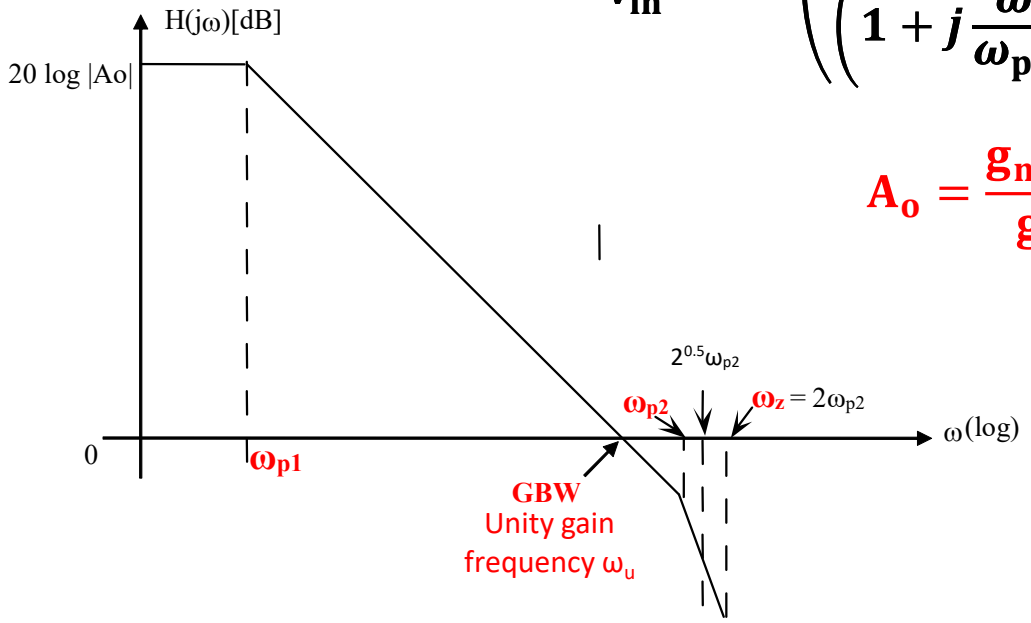
Dom. Pole

$$\omega_{p1} = \frac{g_o}{C_L}$$
$$\omega_{p2} = \frac{g_{m3,4}}{C_3}$$
$$\omega_z = \frac{2g_{m3,4}}{C_3}$$

$$\text{GBW} = A_o\omega_{p1} = \frac{g_{m1,2}}{C_L}$$

Bode Plot

$$\mathbf{H(s)} = \frac{\mathbf{v_{out}}}{\mathbf{v_{in}}} = A_o \left(\frac{1 + j\frac{\omega}{\omega_z}}{\left(1 + j\frac{\omega}{\omega_{p1}}\right)\left(1 + j\frac{\omega}{\omega_{p2}}\right)} \right)$$



$$\mathbf{A_o} = \frac{\mathbf{g_{m1,2}}}{\mathbf{g_o}}$$

$\omega_{p1} = \frac{g_o}{C_L}$: dominant pole

$\omega_{p2} = \frac{g_{m3,4}}{C_3}$: non-dominant pole

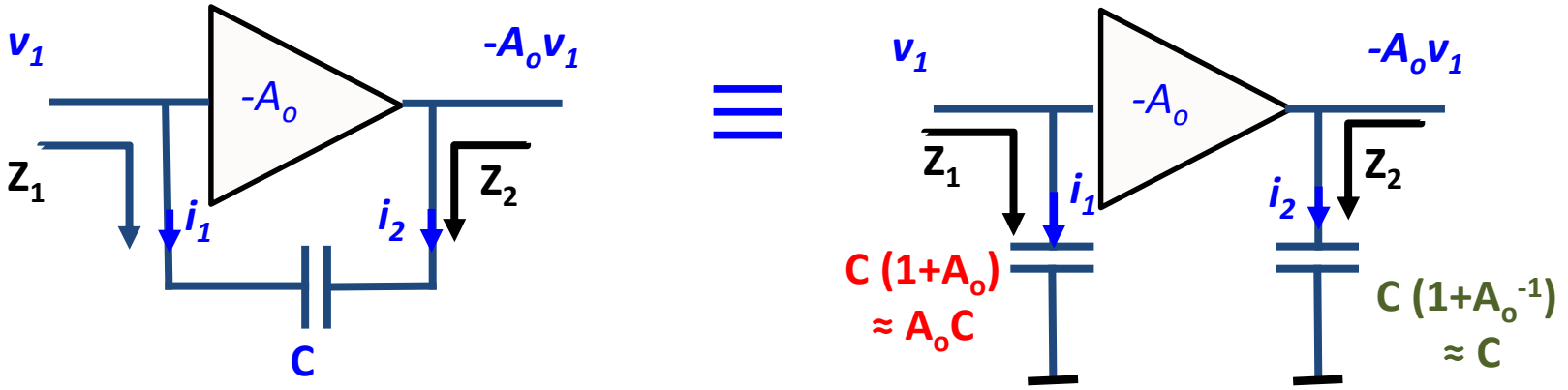
$\omega_z = 2\omega_{p2} = \frac{2g_{m3,4}}{C_3}$: zero

$$\omega_u = \omega_{GBW} = A_o\omega_{p1} = \frac{g_{m1,2}}{C_L}$$

$$Ph(H(j\omega)) \approx Arctg\,(\omega/\omega_z) - Arctg\,(\omega/\omega_{P1}) - arctg\,(\omega/\omega_{p2})$$

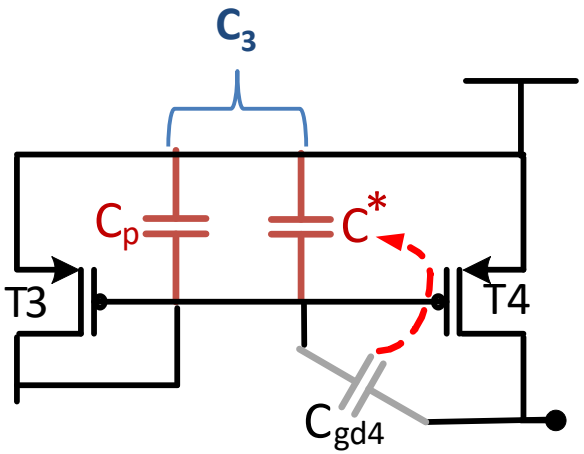
Miller Effcet

- the Miller effect accounts for the increase in the equivalent input capacitance of an inverting voltage amplifier due to amplification of the effect of capacitance between the input and output terminals.



$$Z_1 = \frac{v_1}{i_1} = \frac{v_1}{\frac{v_1 + A_o v_1}{Z_C}} = \frac{1}{j\omega C(1 + A_o)} \qquad Z_2 = \frac{-A_o v_1}{i_2} = \frac{-A_o v_1}{\frac{-A_o v_1 - v_1}{Z_C}} = \frac{1}{j\omega C\left(1 + A_0^{-1}\right)}$$

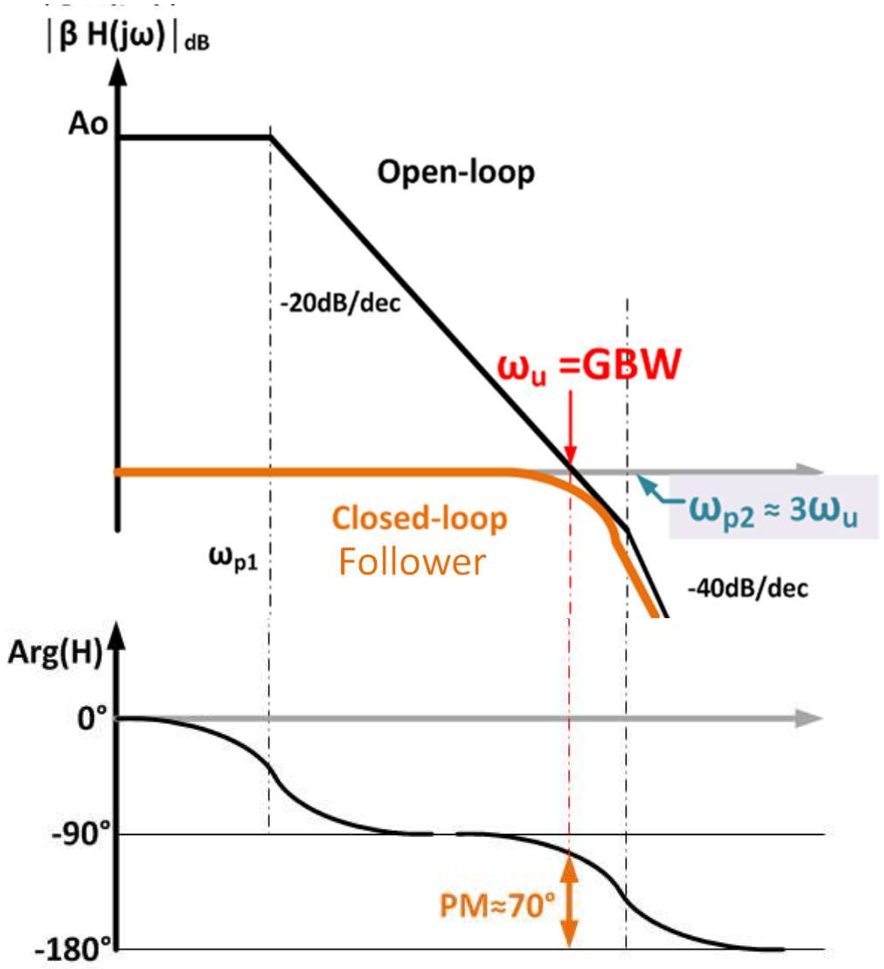
ω_{p2} = ? : Miller effect



- $C_p \approx C_{gs3} + C_{gs4} \approx 2\frac{2}{3} C_{ox} W_3 L_3$
- $C^* \approx A_{T4}\ C_{gd4} \approx \frac{g_{m4}}{g_o}\ C_{gd4} \approx \frac{g_{m4}}{g_o}\ W_4 C_{gd.ov}$
- $C_3 = C_p + C^*$

$$\omega_{p2} = \frac{g_{m3,4}}{C_3} = \frac{g_{m3,4}}{\frac{4}{3} C_{ox} W_3 L_3 + \frac{g_{m4}}{g_o} W_3 C_{gd.ov}}$$

OTA stability



$$H(s) = \frac{v_{out}}{v_{in}} = A_o \left(\frac{1 + j\frac{\omega}{\omega_z}}{\left(1 + j\frac{\omega}{\omega_{p1}}\right)\left(1 + j\frac{\omega}{\omega_{p2}}\right)} \right)$$

Phase Margin for stability

PM = Ph(H($j\omega_{GBW}$))-(-180) ≈

arctg (ω_{GBW}/ω_z) → ≈0° ($\omega_{GBW} << \omega_z$)

- arctg (ω_{GBW}/ω_{P1}) → ≈-90°($\omega_{p1} << \omega_{GBW}$)

- arctg (ω_{GBW}/ω_{p2}) ≈ ?

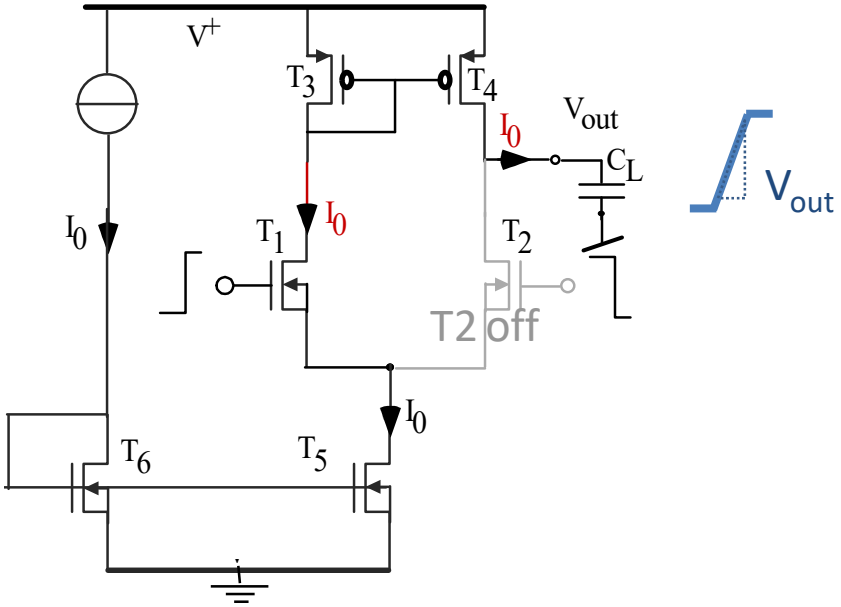
+ 180

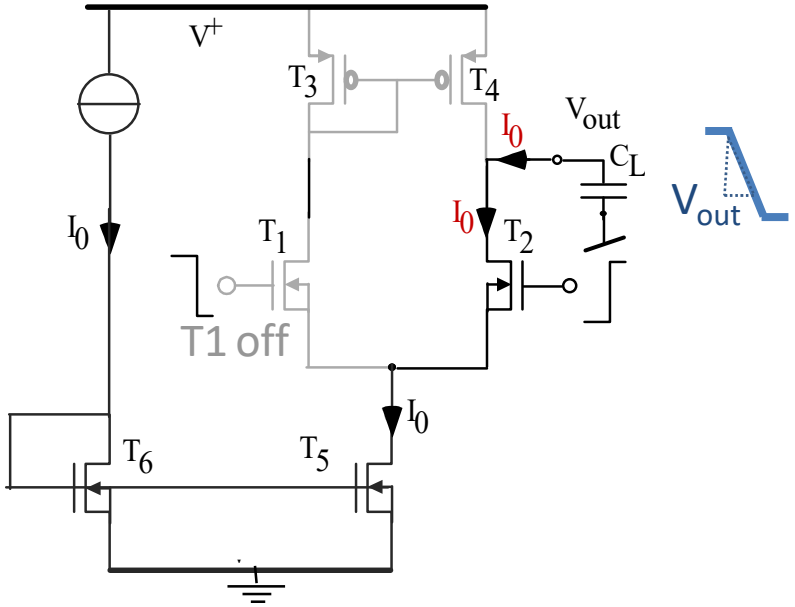
(Stability over PVT variation) → Phase-Margin PM ≈ 60 °-70° → $\omega_{p2} \approx 3\ \omega_{GBW}$

$$\equiv \frac{g_{m3,4}}{C_3} \geq 3\frac{g_{m1,2}}{C_L}$$

OTA-Slew Rate

- Slew Rate (Sr) ≡ maximum rate of change possible for the output voltage
- Sr limited by the currents charging and discharging the capacitors of Amps.





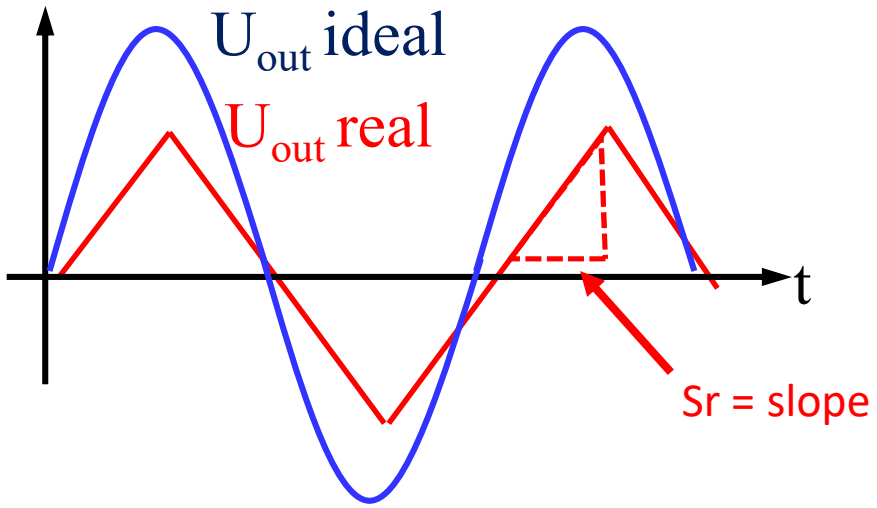
$$Sr = \frac{dV_{out}}{dt} = \frac{I_0}{C_L} \qquad GBW = \frac{g_{m1}}{C_L} = \frac{g_{m1}}{I_0}\frac{I_0}{C_L} \qquad \frac{GBW}{Sr} = \frac{g_{m1}}{I_0} = \frac{1}{2}\frac{g_{m1}}{I_{D1}}$$

During OTA design: usually, Sr gives I_0 and GBW gives g_m

Slew Rate consequences

- Ex: $U_{out} = \hat{U}_{out} \sin(\omega t) \rightarrow (dU_{out}/dt)_{max} = \hat{U}_{out}\, \omega$

If $\hat{U}_{ou}\, \omega > Sr$
→ large signal mode → Speed limited by Sr
i.e. distortion occurs even if $\omega < \omega_{BW}$



Circuit Level Tradeoffs

Consumption/Speed	$I_0 V_{DD} = S_R . C_L . V_{DD}$
Gain / BW	$GBW = g_m / (2\pi C_L)$
$I_{F,diff}$	$\frac{g_m}{I_D} = \frac{1}{nU_T} \cdot \frac{2}{1+\sqrt{4I_F+1}}$
Size	$I_F = \frac{I_D}{I_s} = \frac{I_D}{2n\mu C_{ox} \frac{W}{L} U_T^2}$
DC Gain	$g_m R_{out} = g_m / I_D . [(L_n U_{an})^{-1} + (L_p U_{ap})^{-1}]^{-1}$
Stability	$\frac{g_{m,mir}}{C_{mir}} \geq 3 \frac{g_{m,diff}}{C_L}$
Noise & Offset	….